Amendments to the Specification:

Please replace Paragraph [0025] with the following amended context:

As shown in Fig.5, using the pad nitride layer 28 as an etching stop layer, a dry etching is performed to etch the silicon spacer layer 30 above the pad nitride layer 28 and the silicon spacer layer 30 deposited on the top surface of Poly1. The dry etching continues to etch the node dielectric layer 14 above the pad nitride layer 28 and then etch Poly1 to a second depth d_2 inside the deep trench 11. According to the preferred embodiment of this invention, the second depth d_2 ranges between 800 and 1500 angstroms, more preferably 1000 angstroms. The remaining silicon spacer layer 30 now becomes a silicon spacer 301 on sidewall of the deep trench 11 for protecting the node dielectric layer 14. Subsequently, a wet etching is carried to remove the ~~nde~~ node dielectric layer 14 that is not covered by the silicon spacer 301, thereby exposing the silicon surface at the neck 40 (the interval between second depth d_2 and first depth d_1) of the deep trench 11. As best seen in Fig.5, the node dielectric layer 14 is now divided into an upper dielectric section 141 and a lower dielectric section 142. The upper dielectric section 141 is used to protect the pad oxide layer 26 around the top of the deep trench 11. The lower dielectric section 142 serves as the capacitor dielectric of the deep trench capacitor. At this phase, the surface of the silicon spacer 301, the neck silicon surface of the deep trench, and a top surface 22 of Poly1 constitute a second recess 55.

Please replace Paragraph [0027] with the following amended context:

As shown in Fig.7, a wet etching such as diluted HF is used to remove the silicon oxide layer 60 inside the deep trench 11, thereby forming a bottle-shaped expanded structure 75 having a width w_2 at the neck 40 of the deep trench 11. In accordance with the preferred embodiment of this invention, in a case that the node dielectric layer 14 is ONO dielectric, the upper dielectric section 141 now becomes nitride-oxide (NO) dielectric spacer [[141"]] 141'. It is one of the main features of the present invention that

when wet etching the collar oxide layer 54, the pad oxide layer 26 around the top of the deep trench is protected by the upper section node dielectric 56.

Please replace Paragraph [0028] with the following amended context:

Next, as shown in Fig.8, collar oxide formation begins. A CVD process is performed to deposit a conformal silicon dioxide layer on the interior surface of the deep trench 11. The conformal silicon dioxide layer covers the dielectric spacer [[141"]] 141', the recessed sidewall surface at the expanded neck 40 and the top surface of Poly1. A dry etching is then carried out to etch the conformal silicon dioxide layer, thereby forming a collar oxide layer 80. The dry etching stops when Poly1 is exposed.

Please replace Paragraph [0029] with the following amended context:

As shown in Fig.9, a second polysilicon deposition and recess process is carried out to form a second polysilicon layer (Poly2) atop the first polysilicon layer (Poly1) inside the deep trench 11. The second polysilicon deposition and recess process includes the steps of filling the deep trench and the bottle-shaped structure with a layer of doped polysilicon, followed by etching back the doped polysilicon to a third depth d_3 below the main surface 11 of the substrate 10. According to the preferred embodiment of this invention, the third depth d_3 approximately equals to the first depth d_1. Thereafter, a wet etching such as diluted HF is used to remove the collar oxide layer 80 inside the deep trench 11, which is not covered by the second polysilicon layer (Poly2). The dielectric spacer [[141"]] 141' is then removed by wet etching.